

Notice of References Cited

Application/Control No.

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Applicant(s)/Patent Under
Reexamination
OCHI ET AL.

Examiner

Morella I Rosales-Hanner

Art Unit

2128

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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,009,249	12-1999	Weber, Larren Gene	716/5
	B	US-5,416,717	05-1995	Miyama et al.	703/14
	C	US-6,374,205	04-2002	Kuribayashi et al.	703/14
	D	US-5,867,399	02-1999	Rostoker et al.	716/18
	E	US-6,311,309	10-2001	Southgate, Timothy J.	716/1
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	P.M. Maurer; "Efficient Simulation for Hierarchical and Partitioned Circuits"; VLSI Design 1999; Proc. 12th Int. Conf. 7-10 Jan 1999; Pgs 236-241□□
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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